WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device, which comprises the steps of:

forming a gate line on a semiconductor substrate;

forming a buffer layer and a spacer nitride film on the entire surface of the substrate including the gate line;

selectively etching the buffer layer and the spacer nitride film in such a manner that they remain on both sides of the gate line;

performing an ion implantation process using the remaining buffer layer and spacer nitride film as a barrier film to form junction regions in the semiconductor substrate at both sides of the gate line;

forming an interlayer insulating film on the entire upper portion of the resulting substrate;

selectively removing the interlayer insulating film to form contact holes exposing the upper surface of the junction regions; and

forming contact plugs in the contact holes.

2. The method of Claim 1, which additionally comprises the step of subjecting the entire upper portion of the substrate including the junction regions to a rapid thermal

annealing (RTA) process, before the step of forming the interlayer insulating film.

3. The method of Claim 2, wherein the buffer layer is in the form of a laminated structure of an oxide film and a nitride film, a single-layered oxide film, or a single-layered nitride film.

4. The method of Claim 2, wherein the spacer nitride film is formed to a thickness of 100-700 Å.

5. The method of Claim 2, wherein the ion implantation process is performed using a given tilt angle and a given number of rotations.

6. The method of Claim 5, wherein the tilt angle is 0 to 30 ° and the number of rotations is 2 to 4.

7. The method of Claim 2, wherein the ion implantation process is performed in one time without tilt angle.

8. The method of Claim 1, which additionally comprises the step of performing a rapid thermal annealing (RTA) process after the step of forming the interlayer insulating

film.

9. The method of Claim 1, which additionally comprises the step of subjecting the interlayer insulating film to a reflow annealing process and a rapid thermal annealing process after the step of forming the interlayer insulating film.

10. The method of Claim 1, which additionally comprises the step of performing a high temperature rapid thermal annealing process before forming the contact plugs, and the step of a low temperature rapid thermal annealing process after forming the contact plugs.

11. The method of any of Claim 8, 9 and 10, wherein the buffer layer is in the form of a laminated structure of an oxide film and a nitride film, a single-layered oxide film, or a single-layered nitride film.

12. The method of any of Claim 8, 9 and 10, wherein the spacer nitride film is formed to a thickness of more than 90 Å.

13. The method of any of Claim 8, 9 and 10, wherein

the ion implantation process is performed using a given tilt angle and a given number of rotations.

14. The method of Claim 13, wherein the tilt angle is 0 to 30 ° and the number of rotations is 2 to 4.

15. The method of Claim 8, 9 and 10, wherein the ion implantation process is performed in one time without tilt angle.